IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. To Be Assigned
SENTER BRASHEARS et al.	Art Unit: To Be Assigned
Appl. No.	Examiner: To Be Assigned
Filed: Herewith	Atty. Docket: SP036.C10 (1397.012000A)

For: **System And Method For Handling Load And/Or Store Operations In A Superscalar Microprocessor**

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1.   Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2.   Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed **within three months of the date of filing of a national application** other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3.   Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a.   Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to

the filing of this Information Disclosure Statement.   37 C.F.R.
§ 1.97(e)(1).

☐ b.   Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c.   Attached is our PTO-2038 Credit Card Payment Form **[OR]** Check No. _____ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4.   Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee.   Attached is our PTO-2038 Credit Card Payment Form **[OR]** Check No. _____ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a.   Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.   37 C.F.R. § 1.97(e)(1).

☐ b.   Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
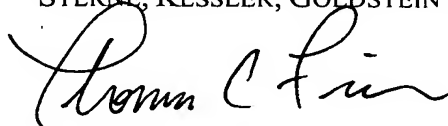
☐ 5.   The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6.   A concise explanation of the relevance of the non-English language document(s) appears below:

☒ 7.   Copies of the documents **except AB13, AC13 and AD13** were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 09/336,589, filed June 21, 1999, which is relied upon for an earlier filing date under 35 U.S.C. § 120. **Copies of documents AB13, AC13 and AD13 are attached. Copies of all other documents, previously submitted are not attached.** 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Thomas C. Fiala
Attorney for Applicants
Registration No. 43,610

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FORM PTO-1449	ATTY. DOCKET NO. SP036.C10		APPLICATION NO. To Be Assigned
INFORMATION DISCLOSURE STATEMENT	APPLICANT: SENTER BRASHEARS et al.		
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	3,346,851	10/1967	Thornton *et al.*			
	AB1	3,541,528	11/1970	Randell			
	AC1	3,771,138	11/1973	Celtruda *et al.*			
	AD1	3,789,365	01/1974	Jen *et al.*			
	AE1	3,916,388	10/1975	Shimp *et al.*			
	AF1	4,034,349	07/1977	Monaco *et al.*			
	AG1	4,084,235	04/1978	Hirtle			
	AH1	4,189,768	02/1980	Liptay *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI1	0 479 390 B1	04/1992	EPO			Yes No
	AJ1	0 426 393 B1	05/1991	EPO			Yes No
	AK1	0 419 105 A2/A3	03/1991	EPO			Yes No
	AL1	0 402 856 B1	12/1990	EPO			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	1	8-Bit Embedded Controller Handbook, Intel, 1989, pp. 1-1 thru 1-19 and 3-1 thru 3-37.
	AN	1	Acosta, Ramón D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, Vol. C-35, No. 9, September 1986, pp. 815-828.
	AO	1	Agerwala *et al.*, "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.
	AR	1	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," pp. 221-235.
	AS	1	Andrews, W., "Distinctions Blur Between DSP Solutions," *Computer Design*, Vol. 28, No. 9, May 1, 1989, Littleton, Mass., pp. 86-99.

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	AA2	4,189,772	02/1980	Liptay			
	AB2	4,200,927	04/1980	Hughes *et al.*			
	AC2	4,228,495	10/1980	Bernhard *et al.*			
	AD2	4,236,206	11/1980	Strecker *et al.*			
	AE2	4,296,470	10/1981	Fairchild *et al.*			
	AF2	4,315,314	02/1982	Russo			
	AG2	4,317,170	02/1982	Wada *et al.*			
	AH2	4,396,982	08/1983	Wada *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI2	0 377 991 A2/A3	07/1990	EPO			Yes No
	AJ2	0 372 751 A2/A3	06/1990	EPO			Yes No
	AK2	0 368 332 B1	05/1990	EPO			Yes No
	AL2	0 354 585 B1	02/1990	EPO			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	2	Bakoglu, H.B. *et al.*, "IBM Second-Generation RISC Machine Organization", *1990 IEEE*, pp. 173-178.
	AN	2	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, Vol. 14, September 1981, pp. 18-27.
	AO	2	Colwell, R.P. *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, Oct. 5-8, 1987, California, pp. 180-192.
	AR	2	Crawford, J., "The Execution Pipeline of the Intel i486 CPU," *IEEE*, 1990, pp. 254-258.
	AS	2	Faix, M. and Schuenemann, C., "Combined Macro/Micro Program Machine," *IBM Technical Disclosure Bulletin*, Vol. 14, No. 1, June 1971, p. 298.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	4,410,939	10/1983	Kawakami			
	AB3	4,434,461	02/1984	Puhl			
	AC3	4,454,578	06/1984	Matsumoto *et al.*			
	AD3	4,456,955	06/1984	Yanagita *et al.*			
	AE3	4,459,657	07/1984	Murao			
	AF3	4,476,525	10/1984	Ishii			
	AG3	4,514,803	04/1985	Agnew *et al.*			
	AH3	4,569,016	02/1986	Hao *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI3	0 171 595 B1	02/1986	EPO			Yes No
	AJ3	0 136 179 A2	04/1985	EPO			Yes No
	AK3	2 575 564	07/1986	FR			Yes No
	AL3	2 011 682 A	07/1979	GB			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	3	Foster *et al.*, "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Trans. On Computers*, December 1971, pp. 1411-1415.
	AN	3	Garth, S.C.J., "Combining RISC and CISC in PC Systems," *IEEE*, pp. 10/1-10/5.
	AO	3	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," *ACM*, 1988, pp. 442-452.
	AR	3	Gross *et al.*, "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, October 5-7, 1982, pp. 114-120.
	AS	3	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," *IEEE*, 1989, pp. 134-137.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	4,587,612	05/1986	Fisk *et al.*			
	AB4	4,626,989	12/1986	Torii			
	AC4	4,654,781	03/1987	Schwartz *et al.*			
	AD4	4,675,806	06/1987	Uchida			
	AE4	4,714,994	12/1987	Oklobdzija *et al.*			
	AF4	4,722,049	01/1988	Lahti			
	AG4	4,734,852	03/1988	Johnson *et al.*			
	AH4	4,739,471	04/1988	Baum *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI4	0 170 398 A3	02/1986	EPO			Yes No
	AJ4	0 272 198 A2	06/1988	EPO			Yes No
	AK4	0 380 854 A3	08/1990	EPO			Yes No
	AL4	2 230 116 A	10/1990	GB			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	4	Heath, S., "Architectural considerations for a M88000 superscalar RISC processor," pp. 6/1-6/6.
	AN	4	Hennessy *et al.*, <u>Computer Architecture: A Quantitative Approach</u>, Morgan Kaufmann Publishers, Inc., 1990 (in its entirety).
	AO	4	Horst, R.W. *et al.*, "Multiple Instruction Issue in the NonStop Cyclone Processor," *IEEE*, 1990, pp. 216-226.
	AR	4	Hwu *et al.*, "Checkpoint Repair for High-Peformance Out-of-Order Execution Machines," *IEEE Trans. On Computers*, Vol. C-36, No. 12, December 1987, pp. 1496-1514.
	AS	4	Hwu *et al.*, "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 45-53.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5	4,739,472	04/1988	Hayashi			
	AB5	4,752,873	06/1988	Shonai et al.			
	AC5	4,758,948	07/1988	May et al.			
	AD5	4,760,519	07/1988	Papworth et al.			
	AE5	4,766,566	08/1988	Chuang			
	AF5	4,771,376	09/1988	Kamiya			
	AG5	4,777,592	10/1988	Yano			
	AH5	4,807,115	02/1989	Torng			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI5	0 461 257 A1	12/1991	EPO			Yes, No
	AJ5	0 473 420	03/1992	EPO			Yes No
	AK5	0 147 775	07/1985	EPO			Yes No
	AL5	3 603 240	08/1987	DE			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	5	Hwu et al., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," *Proceedings from ISCA-13*, Tokyo, Japan, June 2-5, 1986, pp. 297-306.
	AN	5	*i486™ Microprocessor Hardware Reference Manual*, Order No. 240552, Intel Corporation, Santa Clara, California, 1990.
	AO	5	*i486™ Microprocessor Programmer's Reference Manual*, Order No. 240486, Intel Corporation, Santa Clara, California, 1990.
	AR	5	Jelemensky, J. et al., "New Microcomputer Features Advanced Hardware For Real-Time Control Applications," *Electro Conference Record*, Vol. 14, April 11, 1989, Los Angeles, CA, pp. 1-9.
	AS	5	Johnson, M., *Superscalar Microprocessor Design*, Prentice-Hall, Inc., 1991.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6	4,814,976	03/1989	Hansen *et al.*			
	AB6	4,858,105	08/1989	Kuriyama *et al.*			
	AC6	4,897,810	01/1990	Nix			
	AD6	4,901,228	02/1990	Kodama			
	AE6	4,903,196	02/1990	Pomerene *et al.*			
	AF6	4,924,376	05/1990	Ooi			
	AG6	4,926,323	05/1990	Baror *et al.*			
	AH6	4,942,520	07/1990	Langendorf			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI6	0 259 095	03/1988	EPO			Yes No
	AJ6	0 272 198	06/1988	EPO			Yes No
	AK6	0 302 999	02/1989	EPO			Yes No
	AL6	0 377 990	07/1990	EPO			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	6	Johnson, William M., <u>Super-Scalar Processor Design</u>, (Dissertation), Copyright 1989, 134 pages.
	AN	6	Jouppi *et al.*, "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, April 1989, pp. 272-282.
	AO	6	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," *IEEE*, 1989, pp. 229-232.
	AR	6	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," *IEEE Transactions on Computers*, Vol. 38, No. 12, December 1989, pp. 1645-1658.
	AS	6	Keller, R.M., "Look-Ahead Processors," *Computing Surveys*, Vol. 7, No. 4, December 1975, pp. 177-195.

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	AA7	4,942,525	07/1990	Shintani *et al.*			
	AB7	4,985,825	01/1991	Webb, Jr. *et al.*			
	AC7	4,992,931	02/1991	Hirasawa			
	AD7	4,992,934	02/1991	Portanova *et al.*			
	AE7	4,992,938	02/1991	Coke *et al.*			
	AF7	5,003,462	03/1991	Blaner *et al.*			
	AG7	5,051,940	09/1991	Vassiliadis *et al.*			
	AH7	5,075,849	12/1991	Kuriyama *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI7	0 436 092	07/1991	EPO			Yes No
	AJ7	0 465 321 A2	01/1992	EPO			Yes No
	AK7	GB 2 241 801	09/1991	United Kingdom			Yes No
	AL7	JP 2-148238	06/1990	Japan			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	7	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," *Annu. Rev. Comput. Sci.*, Vol. 4, 1990, pp. 173-201.
	AN	7	Lee, R.B., "Precision Architecture," *COMPUTER*, January 1989, pp. 78-91.
	AO	7	McGeady, S., "The i960CA Superscalar Implementation of the 80960 Architecture", *1990 IEEE*, pp. 232-240.
	AR	7	McNeley, K.J. and Milutinovic, V.M., "Emulating a Complex Instruction Set Computer with a Reduced Instruction Set Computer," *IEEE Micro*, Vol. 7, No. 1, pp. 60-71, February 1987.
	AS	7	Melear, C., "The Design of the 88000 RISC Family," *IEEE MICRO*, Vol. 9, No. 2, April 1989, Los Alamitos, CA, pp. 26-38.

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	AA8	5,101,341	03/1992	Circella *et al.*			
	AB8	5,127,091	06/1992	Boufarah *et al.*			
	AC8	5,133,072	07/1992	Buzbee			
	AD8	5,133,077	07/1992	Karne *et al.*			
	AE8	5,148,528	09/1992	Fite *et al.*			
	AF8	5,148,536	09/1992	Witek *et al.*			
	AG8	5,155,843	10/1992	Stamm *et al.*			
	AH8	5,168,571	12/1992	Hoover *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI8	JP 4-77925	03/1992	Japan			Yes No
	AJ8	JP 4-219825	08/1992	Japan			Yes No
	AK8	JP 58-217054	12/1983	Japan			Yes No
	AL8	JP 59-154548	09/1984	Japan			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AM	8	Murakami, K. *et al.*, "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," *ACM*, 1989, pp. 78-85.
AN	8	Nakano, H. *et al.*, "A 80 Mflops 64-bit Microprocessor for Parallel Computer", *IEEE 1991 Custom Integrated Circuits Conference*, pp. 15.2.1-15.2.4.
AO	8	Odnert, D. *et al.*, "Architecture and Compiler Enhancements for PA-RISC Workstations," *Proceedings from IEEE Compcon*, February 25 - March 1, 1991, San Francisco, CA, pp. 214-218.
AR	8	Ohr, S., "Superlong instructions help supermini refine number crunching," *Electronic Design*, Vol. 33, No. 26, November 1985.
AS	8	"Overlap of Store Multiple Operation With Succeeding Operations Through Second Set of General Purpose Registers," *IBM Technical Disclosure Bulletin*, Vol. 28, No. 6, November 1989, New York, NY, pp. 2727-2728.

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	AA9	5,185,868	02/1992	Tran			
	AB9	5,193,206	03/1993	Mills			
	AC9	5,226,126	07/1993	McFarland *et al.*			
	AD9	5,230,068	07/1993	Van Dyke *et al.*			
	AE9	5,251,306	10/1993	Tran			
	AF9	5,317,740	05/1994	Sites			
	AG9	5,323,489	06/1994	Bird			
	AH9	5,355,460	10/1994	Eickenmeyer *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI9	61-33546	02/1986	Japan			Yes No
	AJ9	1-286030	11/1989	Japan			Yes No
	AK9	2-130634	05/1990	Japan			Yes No
	AL9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	9	*Patent Abstracts of Japan*, Vol. 017, No. 082 (P-1489), February 18, 1993.
	AN	9	*Patent Abstracts of Japan*, Vol. 017, No. 084 (P-1490), February 19, 1993.
	AO	9	*Patent Abstracts of Japan*, Vol. 009, No. 006 (P-326), January 11, 1985.
	AR	9	*Patent Abstracts of Japan*, Vol. 010, No. 089, April 1986, & JP, A, 60 225 943 (Hitachi Seisakusho K K) 11 November 1985.
	AS	9	Patt *et al.*, "Critical Issues Regarding HPS, A High Performance Microarchitecture," *Proceedings of the 18th Annual Workshop on Microprogramming*, December 1985, pp. 109-116.

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449	ATTY. DOCKET NO. SP036.C10	APPLICATION NO. To Be Assigned
INFORMATION DISCLOSURE STATEMENT	APPLICANT: SENTER BRASHEARS et al.	
	FILING DATE: Herewith	GROUP: To Be Assigned

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10	5,371,684	12/1994	Iadonato et al.			
	AB10	5,390,355	02/1995	Horst			
	AC10	5,442,757	08/1995	McFarland et al.			
	AD10	5,487,156	01/1996	Popescu et al.			
	AE10	5,539,911	07/1996	Nguyen et al.			
	AF10	5,557,763	09/1996	Senter et al.			
	AG10	5,561,776	10/1996	Popescu et al.			
	AH10	5,574,927	11/1996	Scantlin			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI10						Yes No
	AJ10						Yes No
	AK10						Yes No
	AL10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	10	Patt et al., "HPS, A New Microarchitecture: Rationale and Introduction," *Proceedings of the 18th Annual Workshop on Microprogramming*, December 1985, pp. 103-108.
	AN	10	Pleszkun et al., "The Performance Potential of Multiple Functional Unit Processors," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 37-44.
	AO	10	Pleszkun et al., "WISQ: A Restartable Architecture Using Queues," *Proceedings of the 14th International Symposium on Computer Architecture*, June 1987, pp. 290-299.
	AR	10	Popescu, V. et al., "The Metaflow Architecture," *IEEE Micro*, June 1991, pp. 10-13 & 63-73.
	AS	10	Smith, M.D. et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," *IEEE*, 1990, pp. 344-354.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA11	5,592,636	01/1997	Popescu et al.			
	AB11	5,606,676	02/1997	Grochowski et al.			
	AC11	5,619,668	04/1997	Zaidi			
	AD11	5,625,837	04/1997	Popescu et al.			
	AE11	5,627,983	05/1997	Popescu et al.			
	AF11	5,651,125	07/1997	Witt et al.			
	AG11	5,659,782	08/1997	Senter et al.			
	AH11	5,689,720	11/1997	Nguyen et al.			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AI11						Yes No
	AJ11						Yes No
	AK11						Yes No
	AL11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	11	Smith et al., "Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, June 1985, pp. 36-44.
	AN	11	Smith, J.E. et al., "Implementing Precise Interrupts in Pipelined Processors," *IEEE Transactions on Computers*, Vol. 37, No. 5, May 1998, pp. 562-573.
	AO	11	Smith et al., "Limits on Multiple Instruction Issue," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, April 1989, pp. 290-302.
	AR	11	Sohi et al., "Instruction Issue Logic for High-Performance, Interruptable Pipelined Processors," *14th Annual Int'l Symposium on Computer Architecture*, June 2-5, 1987, pp. 27-34.
	AS	11	Thornton, J.E., <u>Design of a Computer: The Control Data 6600</u>, Control Data Corporation, 1970, pp. 58-140.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA12	5,708,841	01/1998	Popescu et al.			
	AB12	5,768,575	06/1998	McFarland et al.			
	AC12	5,778,210	07/1998	Henstrom et al.			
	AD12	5,797,025	08/1998	Popescu et al.			
	AE12	5,832,205	11/1998	Kelly et al.			
	AF12	5,832,293	11/1998	Popescu et al.			
	AG12	4,839,797	06/1989	Katori et al.			
	AH12	5,233,694	08/1993	Hotta et al.			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI12						Yes No
	AJ12						Yes No
	AK12						Yes No
	AL12						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	12	Tjaden et al., "Detection and Parallel Execution of Independent Instructions," IEEE Trans. On Computers, Vol. C-19, No. 10, October 1970, pp. 889-895.
	AN	12	Tjaden, Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), 1972, pp. 1-199.
	AO	12	Tjaden et al., "Representation of Concurrency with Ordering Matrices," IEEE Trans. On Computers, Vol. C-22, No. 8, August 1973, pp. 752-761.
	AR	12	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," IBM Journal, Vol. 11, January 1967, pp. 25-33.
	AS	12	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," Proceedings of the 19th Annual Hawaii International Conference on System Sciences, 1986, pp. 41-50.

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	FILING DATE: Herewith	GROUP: To Be Assigned

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA13	5,345,569	09/1994	Tran			
	AB13	5,987,593	11/1999	Senter et al.			
	AC13	6,230,254	05/2001	Senter et al.			
	AD13	6,434,693	08/2002	Senter et al.			
	AE13						
	AF13						
	AG13						
	AH13						

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AI13						Yes No
	AJ13						Yes No
	AK13						Yes No
	AL13						Yes NO

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	13	Wedig, R.G., Detection of Concurrency In Directly Executed Language Instruction Streams, (Dissertation), June 1982, pp. 1-179.
	AN	13	Weiss et al., "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from IEEE Trans. on Computers, Vol. C-33, No. 11, November 1984, pp. 1013-1022.
	AO	13	Weiss, R., "Third-Generation RISC Processors," EDN, March 30, 1992, pp. 96-108.
	AR	13	Wharton, J. J., "Parallel 486 pipelines produce peak processor performance," Microprocessor Report, Vol. 3, No. 6, June 1989, p13(5).
	AS	13	IBM Journal of Research and Development, Vol. 34, No. 1, January 1990, pp. 1-70.

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FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP036.C10	APPLICATION NO. To Be Assigned
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	FILING DATE: Herewith	GROUP: To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA14						
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	AJ14						
	AK14						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL14						Yes No
	AM14						Yes No
	AN14						Yes No
	AO14						Yes No
	AP14						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	14	Kuga, M. et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMP (Single Instruction Stream/Multiple Instruction Pipelining) Method," *Transactions of Information Processing Society of Japan*, Information Processing Society of Japan, Vol. 30, No. 12, December 1989, pages 1603-1611.
	AS	14	English-language translation of Kuga, M. et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMP (Single Instruction Stream/Multiple Instruction Pipelining) Method," *Transactions of Information Processing Society of Japan*, Information Processing Society of Japan, Vol. 30, No. 12, December 1989, pages 1603-1624.
	AT	14	Johnson, M., *Superscalar Microprocessor Design*, Prentice Hall, 1991, pages 50-53 and pages 147-163.

EXAMINER	DATE CONSIDERED

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		APPLICANT: SENTER BRASHEARS et al.				
	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	**FILING DATE: Herewith**		**GROUP: To Be Assigned**		

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA15						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL15						Yes No
	AM15						Yes No
	AN15						Yes No
	AO15						Yes No
	AP15						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	15	English-language translation of Japanese Laid-Open Patent Application No. H2-148238, (June 7, 1990 - date of publication), 15 pages.
	AS	15	English-language translation of Japanese Laid-Open Patent Application No. H4-77925, (March 12, 1992 - date of publication), 33 pages.
	AT	15	English-language translation of Japanese Laid-Open Patent Application No. S58-217054, (December 16, 1983 - date of publication), 18 pages.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA16						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL16						Yes No
	AM16						Yes No
	AN16						Yes· No
	AO16						Yes No
	AP16						Yes No·

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	16	English-language translation of Japanese Laid-Open Patent Application No. S59-154548, (September 3, 1984 - date of publication), 15 pages.
	AS	16	English-language translation of Japanese Laid-Open Patent Application No. S61-33546, (February 17, 1986 - date of publication), 25 pages.
	AT	16	English-language translation of Japanese Laid-Open Patent Application No. H1-286030, (November 17, 1989 - date of publication), 9 pages.

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA17						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL17						Yes No
	AM17						Yes No
	AN17						Yes No
	AO17						Yes No
	AP17						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	17	Notification of Reason for Refusal for Japanese Patent Application No. 1994-509063, mailed August 27, 2002, 3 pages.
	AS	17	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 1994-509063, mailed August 27, 2002, 5 pages.
	AT	17	Notification of Reason for Refusal for Japanese Patent Application No. 2000-008263, mailed August 14, 2002, 3 pages.

EXAMINER	DATE CONSIDERED

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	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	FILING DATE: Herewith	GROUP: To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA18						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL18						Yes No
	AM18						Yes No
	AN18						Yes No
	AO18						Yes No
	AP18						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	18	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-008263, mailed August 14, 2002, 5 pages.
	AS	18	Notification of Reason for Refusal for Japanese Patent Application No. 2000-008266, mailed August 14, 2002, 3 pages.
	AT	18	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-008266, mailed August 14, 2002, 5 pages.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA19						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL19						Yes No
	AM19						Yes No
	AN19						Yes No
	AO19						Yes No
	AP19						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	19	Notification of Reason for Refusal for Japanese Patent Application No. 2000-008267, mailed August 16, 2002, 3 pages.
	AS	19	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-008267, mailed August 16, 2002, 6 pages.
	AT	19	Notification of Reason for Refusal for Japanese Patent Application No. 2000-008268, mailed August 14, 2002, 3 pages.

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U.S. PATENT DOCUMENTS

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	AA20						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL20						Yes No
	AM20						Yes No
	AN20						Yes No
	AO20						Yes No
	AP20						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	20	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-008268, mailed August 14, 2002, 5 pages.
	AS	20	Notification of Reason for Refusal for Japanese Patent Application No. 2000-008271, mailed August 14, 2002, 3 pages.
	AT	20	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-008271, mailed August 14, 2002, 5 pages.

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	AA21						
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	AJ21						
	AK21						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL21						Yes No
	AM21						Yes No
	AN21						Yes No
	AO21						Yes No
	AP21						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	21	English-language translation of Japanese Laid-Open Patent Application No. H2-130634, (May 18, 1990 - date of publication), 56 pages.
	AS	21	
	AT	21	

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